

INTELLIGENT INTERACTIVE SYNTHESIZER

SURFACE MOUNT MODEL: FSH9496-20

OPTIMIZED LOOP PARAMETERS

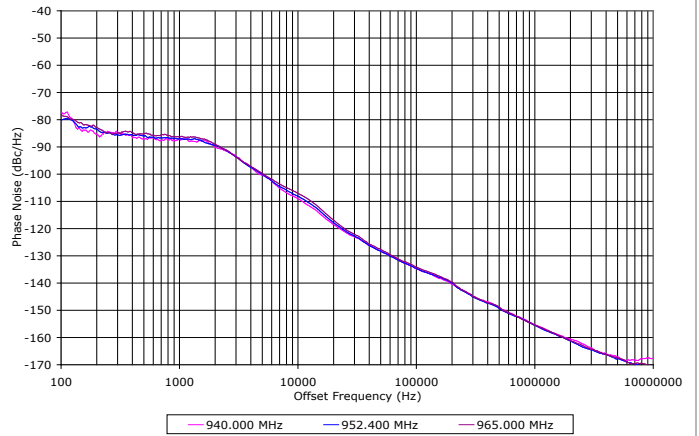
940 - 970 MHz

FEATURES:

- ▶ Exceptionally Low Phase Noise
- ▶ Optimized Reference Sidebands
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount
- ▶ Buffered Output



Phase Noise



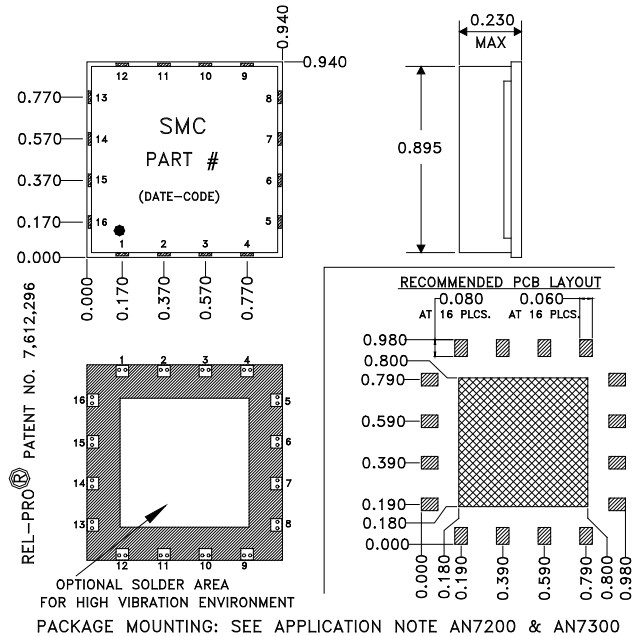
SPECIFICATIONS (Rev. F 03/24/11)

Frequency	940 - 970 MHz		
Step Size	200 kHz		
Reference Input Frequency	10 MHz ¹		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	15
	VCO	+5	50
	Tune	+5	10
Output Power	+5 dBm (Min.)		
Spurious Suppression	80 dB (Typ.)		
Harmonic Suppression	12 dB (Typ.)		
Settling Time	20 mSec (Typ.) ²		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3V		
Typical Phase Noise	Offset	Phase Noise	
	@ 1 kHz	-87 dBc/Hz	
	@ 10 kHz	-109 dBc/Hz	
	@ 100 kHz	-134 dBc/Hz	
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		

¹ Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the factory default setting. 150 MHz (Max.)

² From the rising edge of LE to stable lock detect

Package # 273LF



Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (VCO)	+5.5 V
Bias Voltage (Tune)	+8.0 V
DC Voltage Applied to RF Out	±25 V

Port Configuration

Pin 1,2,3 - NC	Pin 8 - Vcc (Tune)	Pin 16 - Clock In
Pin 4 - Error flag	Pin 9 - Vcc (VCO)	All Others - Ground
Pin 5 - Latch Enable In	Pin 13 - RF Out	
Pin 6 - Ref. In	Pin 14 - Lock Detect Out *	NC - No Connection
Pin 7 - Vcc (Digital)	Pin 15 - Data In	

* High when locked (source/sink 500 uA)

This product is manufactured under one or more of the following patents: Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623 | Pending: 60/493075; 60/501371 & 60/501790; 60/527957 & 60/528670; 60/563481; 60/564173; 60/589090; 60/601823; 60/605791; EV31369834; 11/259766; 60/622485 & 60/710310; 10/937525/60/736901; 60/732787; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 2,563,174; 7,580,693; 7,612,296; 2,524,751

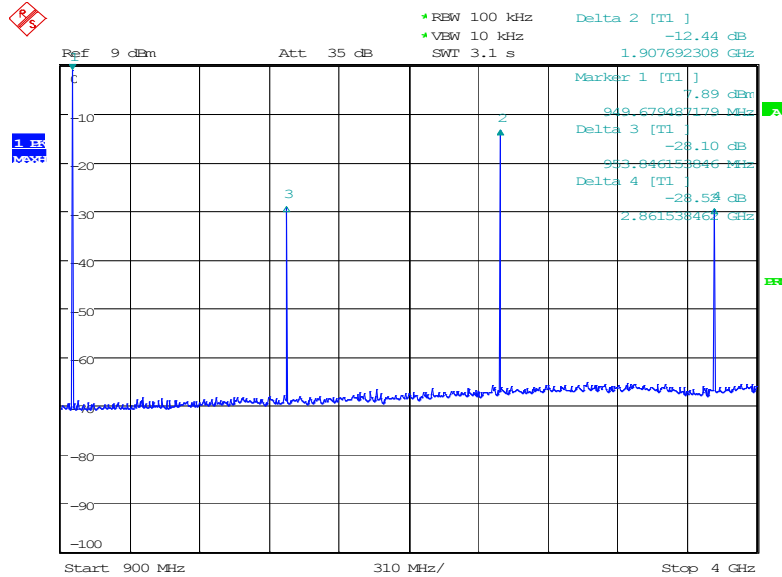
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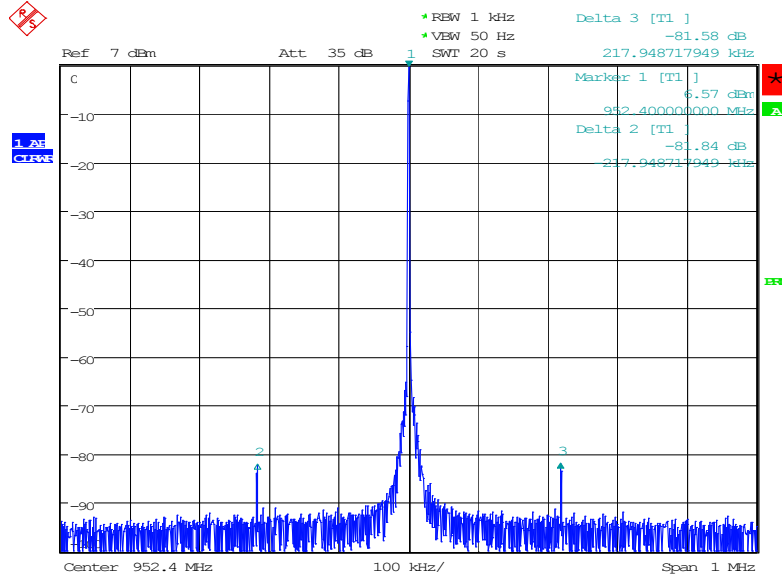
940 - 970 MHz

HARMONIC SUPPRESSION



Date: 21.AUG.2006 16:43:23

REFERENCE SIDEBAND SUPPRESSION



Date: 21.AUG.2006 19:58:02

PERFORMANCE PLOTS

This product is manufactured under one or more of the following patents. Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623
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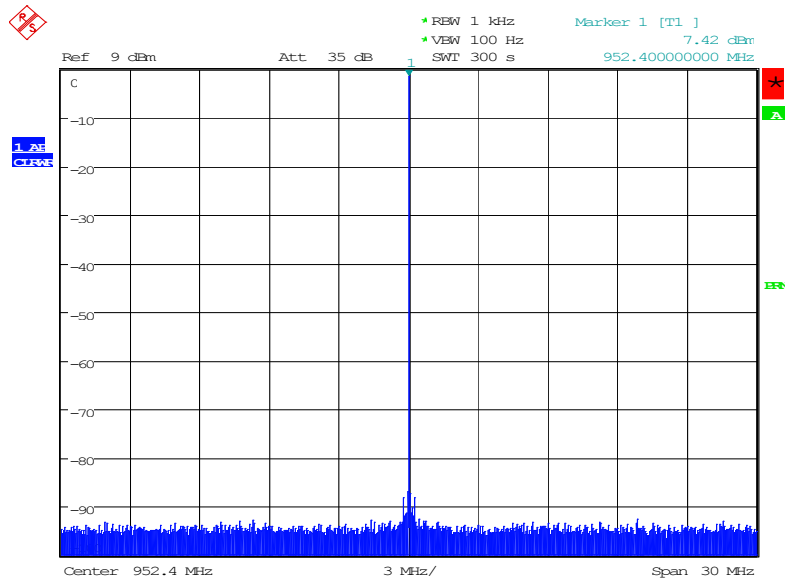
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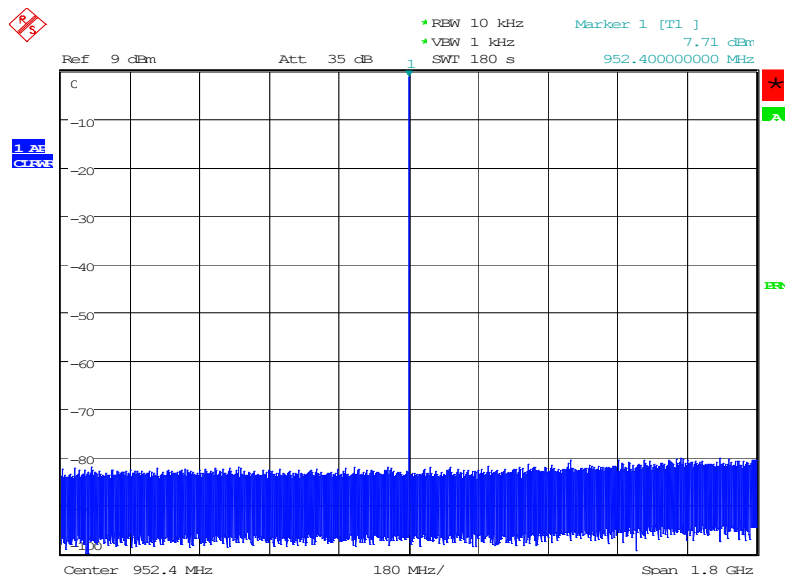
OPTIMIZED LOOP PARAMETERS

940 - 970 MHz

REFERENCE SIDEBAND SUPPRESSION



Date: 21.AUG.2006 17:36:48



Date: 21.AUG.2006 18:06:34

PERFORMANCE PLOTS

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